IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JEFFREY SCOTT ET AL.
Filed:	HEREWITH
For:	DIRECT DIGITAL ACCESS ARRANGEMENT CIRCUITRY AND METHOD FOR CONNECTING TO PHONE LINES
Serial No.:	UNKNOWN
Prior Group Art Unit:	2631
Examiner:	UNKNOWN
Atty Dkt:	SILA:028C4

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Signature

2/17/04
Date

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

PRELIMINARY AMENDMENT

Please amend the application as follows.

In the specification:

On page 1, please replace the paragraph from lines 7-18 to read as follows:

This application is a continuation of U.S. Serial No. 10/227,104 filed on August 23, 2002, entitled "Direct Digital Access Arrangement Circuitry and Method for Connecting to Phone Lines" which is a continuation of U.S. Serial No. 10/127,285 filed

on April 22, 2002, entitled "Direct Digital Access Arrangement Circuitry and Method for Connecting to Phone Lines" which is a continuation of U.S. Serial No. 09/035,175 (now U.S. Patent No. 6,385,235), filed on March 4, 1998, entitled "Direct Digital Access Arrangement Circuitry and Method for Connecting to Phone Lines" which is a continuation-in-part of U. S. Serial Nos. 08/841,409 (now U.S. Patent No. 6,137,827), 08/837,702 (now U.S. Patent No. 5,870,046), and 08/837,714 (now U.S. Patent No. 6,430,229) all filed on April 22, 1997. Further, the following U. S. patent applications filed concurrently herewith Serial No. 09/034,621 (now U.S. Patent No. 6,442,271), entitled "Digital Isolation System With Low Power Mode" by George Tyson Tuttle et al; Serial No. 09/034,456 (now U.S. Patent No. 6,144,326), entitled "Digital Isolation System With ADC Offset Calibration; by Andrew W. Krone et al.; Serial No. 09/034,455 (now U.S. Patent No. 6,480,602), entitled "Ring-Detect Interface Circuitry and Method for a Communication System" by Timothy J. Dupuis et al.; Serial No. 09/035,779 (now U.S. Patent No. 6,389,134), entitled "Call Progress Monitor Circuitry and Method for a Communication System" by Timothy J. Dupuis et al.; Serial No. 09/034,683 (now U.S. Patent No. 6,167,134), entitled "External Resistor and Method to Minimize Power Dissipation in DC Holding Circuitry for a Communication System" by Jeffrey W. Scott et al.; Serial No. 09/034,620 (now U.S. Patent No. 6,160,885), entitled "Caller ID Circuit Powered Through Hookswitch Devices" by Jeffrey W. Scott et al.; and Serial No. 09/034,682 (now U.S. Patent No. 6,408,034), entitled "Framed Delta Sigma Data With Unlikely Delta Sigma Data Patterns" by Andrew W. Krone et al., are expressly incorporated herein by reference.

~~This is a continuation-in-part of U. S. Serial Nos. 08/841,409, 08/837,702 and 08/837,714 all filed on April 22, 1997. Further, the following U. S. patent applications filed concurrently herewith Serial No. _____, entitled "Digital Isolation System With Data Scrambling" by George Tyson Tuttle et al; Serial No. _____, entitled "Digital Isolation With ADC Offset Calibration; by Andrew W. Krone et al.; Serial No. _____, entitled "Ring-Detect Interface Circuitry and Method for a Communication System" by Timothy J. Dupuis et al.; Serial No. _____, entitled "Call Progress Monitor Circuitry and Method for a Communication System" by Timothy J. Dupuis et~~

~~al.; Serial No. _____, entitled "External Resistor and Method to Minimize Power Dissipation in DC Holding Circuitry for a Communication System" by Jeffrey W. Scott et al.; Serial No. _____, entitled "Caller ID Circuit Powered Through Hookswitch Devices" by Jeffrey W. Scott et al.; and Serial No. _____, entitled "Framed Delta Sigma Data With Unlikely Delta Sigma Data Patterns" by Andrew W. Krone et al., are expressly incorporated herein by reference.~~

On page 24, please replace the paragraph from lines 15-31 with the following:

A preferred embodiment of frequency detector 818 is shown in Figure 10. The inputs to frequency detector 818 are the DATA and CK4 signals and the outputs are the SPEED-UP2 and SLOW-DOWN2 signals. Delay cell 880 has its input connected to CK4 and output connected to one input of NOR gate 882. The delay cell 880 consists of an even number of capacitively loaded inverter stages or other delay generating circuitry and is well known in the art. The output of inverter 884 is connected to the other input of NOR gate 882 and the input of inverter 884 is connected to CK4. The output 886 of NOR gate 882 is reset pulse that occurs on the rising edge of CK4, and is connected to the reset input of D flip-flops 888, 890, and 892. The input of inverter ~~894~~ 895 is connected to DATA. The output of inverter ~~894~~ 895 is connected to the clock input of D flip-flops 888, 890, and 892. The D input of flip-flop 888 is connected to V_{DD}. The D-input of flip-flop 890 is connected to the Q-output of flip-flop 888. The D-input of flip-flop 892 is connected to the Q-output of flip-flop 890. D flip-flops 894 and 896 have their clock inputs connected to CK4. The D input of flip-flop 894 is connected to the Q output of flip-flop 888. The D-input of flip-flop 896 is connected to the Q-output of flip-flop 890. The input of inverter 898 is connected to the Q-output of flip-flop 894, and the output of inverter 898 is the SLOW-DOWN2 signal. OR gate 900 provides the SPEED-UP2 signal. One input of OR gate 900 is connected to the Q-output of flip-flop 896, and the other input is connected to the Q-output of flip-flop 892. The SPEED-UP2 and SLOW-DOWN2 signals are connected to the frequency-detector charge pump 824.